

Customer No.: 31561
Docket No.: 9839-US-PA
Application No.: 10/709,603

AMENDMENT

To the Claims:

1. (currently amended) A method of increasing the a cell retention capacity of a silicon nitride read-only-memory, wherein the silicon nitride read-only-memory is formed inside a wafer, the method comprising the step of:

performing a plasma treatment to the wafer, wherein the plasma treatment is last plasma treatment of the wafer;

baking the wafer: and

performing a wafer sort test.

2. (original) The method of claim 1, wherein after performing the last plasma treatment of the wafer but before performing the wafer sort test, furthermore comprises performing an after etch inspection, an alloying process, a wafer acceptance test and a quality control inspection.

3. (original) The method of claim 2, wherein the baking process is carried out after performing the after etch inspection but before the alloying process.

4. (original) The method of claim 2, wherein the baking process is carried out after performing the alloying process but before the wafer acceptance test.

5. (original) The method of claim 2, wherein the baking process is carried out after performing the wafer acceptance test but before the quality control inspection.

6. (original) The method of claim 2, wherein the baking process is carried out after performing the quality control inspection but before the wafer sort test.

Customer No.: 31561
Docket No.: 9839-US-PA
Application No.: 10/709,603

7. (original) The method of claim 1, wherein the wafer sort test comprises a memory cell retention check.

8. (currently amended) The method of claim 7, wherein the baking process is carried out using ~~the same~~ a heating device the same to that for performing the memory cell retention check.

9. (currently amended) A method for increasing ~~the~~ a cell retention capacity of a silicon nitride read-only-memory formed on a wafer, the method comprising the steps of:

forming a passivation layer and a patterned photoresist layer over the wafer;
etching away a portion of the passivation layer using the patterned photoresist layer as a mask;

removing the patterned photoresist layer;

performing an after etch inspection;

performing an alloying process;

performing a wafer acceptance test;

performing a quality control inspection; and

performing a wafer sort test;

wherein one major aspect of the method is to perform the baking process after removing the patterned photoresist layer but before the wafer sort test.

10. (currently amended) The method of claim 9, wherein the patterned photoresist layer is removed by performing a plasma dry etching.

Customer No.: 31561
Docket No.: 9839-US-PA
Application No.: 10/709,603

11. (original) The method of claim 9, wherein the baking process is carried out after performing the after etch inspection but before the alloying process.
12. (original) The method of claim 9, wherein the baking process is carried out after performing the alloying process but before the wafer acceptance test.
13. (original) The method of claim 9, wherein the baking process is carried out after performing the wafer acceptance test but before the quality control inspection.
14. (original) The method of claim 9, wherein the baking process is carried out after performing the quality control inspection but before the wafer sort test.
15. (original) The method of claim 9, wherein the wafer sort test comprises a memory cell retention check.
16. (currently amended) The method of claim 15, wherein the baking process is carried out using ~~the same~~ a heating device the same to that for performing the memory cell retention check.